ABSTRACT OF THE DISCLOSURE

In an image processing apparatus to conduct an on-screen display operation, the bus band of an image memory is minimized. The apparatus includes an image memory including a first memory area to store a first image data group of a first image for a background and a second memory area for storing a second image data group of a second image for an on-screen display, a display buffer memory for storing, in a format to be displayed on a display screen, the first image and the second image read from the image memory; and a control section for controlling accesses in the image memory and the display buffer memory, for reading the first image data group from the first memory area and writing the first image data group in the display buffer memory, and for reading the second image data group from the second memory area and writing the second image data group in a specified area of the display buffer memory. The control section includes a data expansion control section capable of increasing a data amount of the second image data group read from the image memory, according to the second image data group.